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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/490,132	01/24/2000	William C. Moyer	SC10927TS	6776

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EXAMINER

HUYNH, KIM T

ART UNIT

PAPER NUMBER

2181

DATE MAILED: 06/11/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/490,132

Applicant(s)

MOYER, WILLIAM C.

Examiner

Kim Huynh

Art Unit

2181

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). ____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim1-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Chang (U.S Patent 5,057,997)

Chang discloses a method for implementing interrupts in a data processing system (fig.1, 10), comprising the steps of:

- providing a first storage device (fig.1, 13) having a plurality of inputs, each of the plurality of inputs being coupled by a respective physical conductor (fig.1, 14), (col.3, lines 21-24) to one of a plurality of hardware-generated interrupt sources which selectively generate hardware interrupts and selectively storing the hardware interrupts, the first storage device providing one or more hardware-generated interrupt signals (col.3, lines 15-30);
- providing a second storage device (fig.1, 12) having one or more inputs, each of the one or more inputs receiving and storing a predetermined one of a plurality of software-generated interrupt signals, at least some of the predetermined plurality of software-generated interrupt signals indicating an interrupt from a different source or of a different type than the hardware interrupts, the second storage

device providing one or more software-generated interrupt signals (col.3, lines 17-68), (col.4, lines 1-7); and

- coupling logic circuitry (fig.1, 18) to the first storage device and the second storage device for receiving the one or more hardware-generated interrupt signals and the one or more software-generated signals, the logic circuitry providing an interrupt request signal which will cause an interrupt to occur in the data processing system (col.3, lines 15-68).
- assigning an interrupt prioritization level to specific storage locations of the first storage device and the second storage device, the interrupt prioritization level of the plurality of hardware-generated interrupt source coupled to the first storage device being permanently assigned, but assignment of the interrupt prioritization level of interrupt sources associated with the second storage device being variable by software control (col.3, lines 36-68), (col.4, lines 1-13), (col.4, 45-67).
- assigning a portion of the plurality of software-generated interrupt signals stored in the second storage device to represent interrupts from some interrupt sources generating hardware interrupt and having a corresponding interrupt prioritization level (col.3, lines 36-68), (col.4, lines 1-67).
- assigning a portion of the plurality of software-generated interrupt signals stored in the second storage device to represent interrupts from same interrupt sources generating hardware interrupts and having an interrupt prioritization level which differs from the interrupt prioritization level of the plurality of hardware-generated

interrupt sources coupled to the first storage device (col.3, line 36-57), (col.4, lines 1-67).

- changing interrupt servicing from servicing a hardware-generated interrupt and switching to servicing a software-generated interrupt of higher prioritization before completion of servicing of the hardware-generated interrupt occurs (col.2, lines 1-6).
- changing prioritization level of a predetermined hardware-generated interrupt by providing a software-generated interrupt which represents a corresponding hardware-generated interrupt source for the predetermined hardware-generated interrupt but with a different prioritization level than the predetermined hardware-generated interrupt (col.2, lines 1-6), (col.5, lines 27-68).
- determining priority between two interrupts, a first interrupt being hardware-generated and a second interrupt being software-generated, when the two interrupts have a same prioritization level by choosing to service one of the hardware-generated first interrupt or the software-generated second interrupt (col.5, lines 10-68);
- coupling enabling circuitry between the first and second storage devices and the logic circuitry, the enabling circuitry receiving the hardware-generated and software-generated interrupts and determining whether to pass the hardware-generated and software-generated interrupts to the logic circuitry for further processing (col.5, lines 11-26).
- a plurality of hardware interrupt sources (col.3, lines 40-57);

- the hardware interrupt storage device and the software interrupt storage device have an assigned interrupt prioritization level to specific storage locations, the interrupt prioritization level of the hardware interrupt sources being permanently assigned, but assignment of the interrupt prioritization level of interrupt sources associated with the software-generated interrupt signals being variable by software control (col.5, lines 17-35), (col.5, lines 62-68).
- wherein a software-generated interrupt signal of higher priority than a currently executing hardware-generated interrupt signal is provided to the logic circuitry (fig.1, 18) prior to completion of an associated hardware interrupt servicing, and the data processing system suspends processing of the hardware interrupt servicing to process an associated software interrupt servicing (fig.1, 11), (col.3, lines 8-68), (col.5, lines 4-26).
- a mask register coupled to the hardware interrupt storage device and the software interrupt storage device for selectively preventing hardware-generated interrupt signals and software-generated interrupt signals from propagating to the logic circuitry (col.5, lines 50-61).
- wherein the hardware interrupt storage device and the software interrupt storage device are each implemented as latch circuits (col.5, lines 62-68).
- executing software with the data processing system to generate a predetermined software-generated interrupt signal which emulates a predetermined one of the hardware-generated interrupt sources but with a priority which differs from the predetermined one of the hardware-generated interrupt sources, thereby

dynamically changing prioritization of servicing of interrupts in the data processing system (col.6, lines 6-29); and

- generating the predetermined software-generated interrupt signal which emulates the predetermined one of the hardware-generated interrupt sources while another hardware-generated interrupt is being serviced, the predetermined software-generated interrupt signal having a priority which is higher than the other hardware-generated interrupt being serviced; and suspending servicing of the other hardware-generated interrupt being service to begin servicing of the predetermined software-generated interrupt signal (col.5, lines 26-48).
- masking the one or more hardware-generated interrupt signals and the one or more software-generated interrupt signals to selectively pass active interrupt signals to the logic circuitry in response to an enable signal (col.5, lines 50-61).

Conclusion

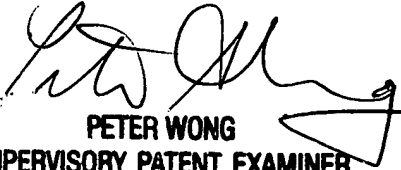
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Wong can be reached on (703)305-3477 or via e-mail addressed to [Peter.Wong@uspto.gov]. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-7249 for regular communications and (703)746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.

Kim Huynh

May 29, 2002


PETER WONG
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